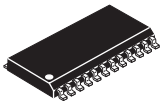
Document Number: MC33291
Rev 5, 07/2008

Eight-Output Switch with Serial Peripheral Interface I/O

33291

LOW-SIDE SWITCH



DW SUFFIX
EG SUFFIX (PB-FREE)
98ASB42344B
24-PIN SOICW

The 33291 device is an eight-output, low-side power switch with 8-bit serial input control. The 33291 is a versatile circuit designed for automotive applications, but is well suited for other environments. The 33291 incorporates SMARTMOS technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs. The 33291 interfaces directly with a microcontroller to control various inductive or incandescent loads.

The circuit's innovative monitoring and protection features include very low standby current, SPI cascade fault reporting capability, internal 53 V clamp on each output, output-specific diagnostics, and independent shutdown of outputs.

The device is parametrically specified over an ambient temperature range of -40°C ≤ T_A ≤ 125°C and 9.0 V ≤ V_{PWR} ≤ 16 V supply.

Features

- Designed to Operate Over Wide Supply Voltages of 5.5 V to 26.5 V
- Interfaces to Microprocessor Using 8-Bit SPI I/O Protocol up to 3.0 MHz
- 1.0 A Peak Current Outputs with Maximum $R_{DS(ON)}$ of 1.6 Ω at T_J - 150°C
- Outputs Current-Limited to Accommodate In-Rush Currents Associated with Switching Incandescent Loads
- Output Voltages Clamped to 53 V During Inductive Switching
- Maximum Sleep Current (I_{PWR}) of 25 µA
- Maximum of 4.0 mA I_{DD} During Operation
- Pb-Free Packaging Designated by Suffix Code EG

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33291DW/R2	-40°C to 125°C	24 SOICW
MCZ33291EG/R2		

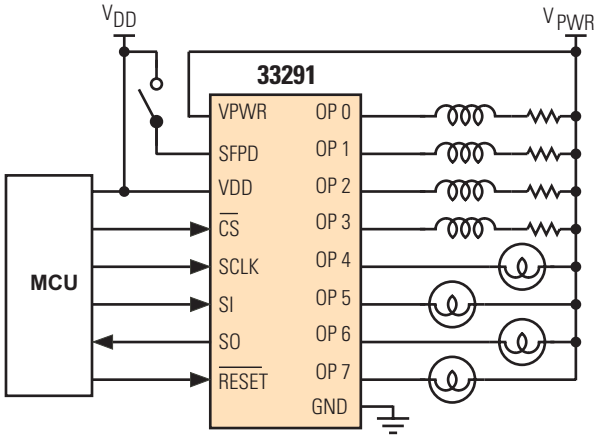


Figure 1. 33291 Simplified Application Schematic

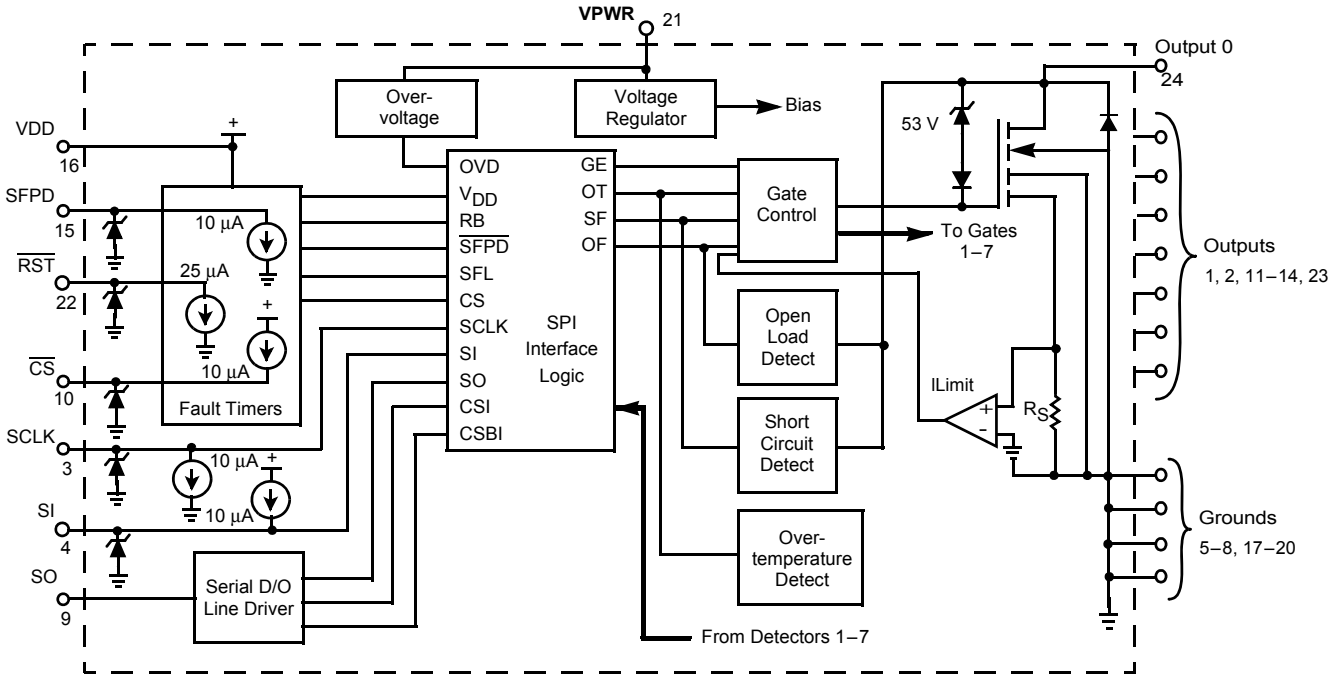


Figure 2. 33291 Simplified Block Diagram

Table 1. Fault Operation

SERIAL OUTPUT (SO) PIN REPORTS

Overvoltage	Overvoltage condition reported.
Overtemperature	Fault reported by Serial Output (SO) pin.
Overcurrent	SO pin reports short to battery/supply or overcurrent condition.
Output ON, Open Load Fault	Not reported.
Output OFF, Open Load Fault	SO pin reports output OFF open load condition.

DEVICE SHUTDOWNS

Overvoltage	Total device shutdown at V_{PWR} = 28 V to 36 V. All outputs are latched off while the SPI register is reset (cleared). Outputs can be turned back on with a new SPI command after V_{PWR} has decayed below 26.5 V.
Overtemperature	Only the output experiencing an overtemperature condition turns OFF.
Overcurrent	Only the output experiencing an overcurrent shuts down at 1.0 A to 3.0 A after a 70 µs to 250 µs delay, with SFPD pin grounded. All other outputs will continue to operate in a current limit mode with no shutdown if the SFPD pin is at 5.0 V (so long as the individual outputs are not experiencing thermal limit conditions).

PIN CONNECTIONS

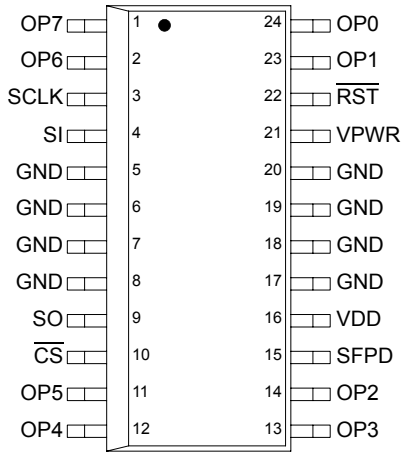


Figure 3. 33291 Pin Connections

Table 2. Pin Definitions

Pin	Pin Name	Formal Name	Definition
1	OP7	Output 7	Connection to drain of output MOSFET number seven.
2	OP6	Output 6	Connection to drain of output MOSFET number six.
3	SCLK	System Clock	Clocks the internal Shift registers of the 33291.
4	SI	Serial Input	This pin is for the input of serial instruction data. SI information is read on the falling edge of SCLK.
5–8, 17–20	GND	Ground	Connection to IC Power Ground and functions as part of heat sinking path.
9	SO	Serial Output	Tri-stateable output from the Shift register.
10	$\overline{CS}$	Chip Select	Whenever this pin is in a logic low state, data can be transferred from the MCU to the 33291 through the SI pin and from the 33291 to the MCU through the SO pin.
11	OP5	Output 5	Connection to drain of output MOSFET number five.
12	OP4	Output 4	Connection to drain of output MOSFET number four.
13	OP3	Output 3	Connection to drain of output MOSFET number three.
14	OP2	Output 2	Connection to drain of output MOSFET number two.
15	SFPD	Short Fault Protect Disable	This pin is used to prevent the outputs from latching-OFF because of an overcurrent condition.
16	VDD	Logic Supply	Plus supply for logic.
21	VPWR	Output MOSFET Gate Drive Supply	Main power supply.
22	$\overline{RST}$	Reset	This pin is active low. It is used to clear the SPI Shift register, thereby setting all output switches OFF.
23	OP1	Output 1	Connection to drain of output MOSFET number one.
24	OP0	Output 0	Connection to drain of output MOSFET number zero.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Power Supply Voltage Normal Operation (Steady-State) Transient Conditions (1)	 $V_{PWR(SUS)}$ $V_{PWR(PK)}$	 -1.5 to 26.5 -13 to 60	V
Logic Supply Voltage (2)	V_{DD}	-0.3 to 7.0	V
Input Pin Voltage (3)	V_{IN}	-0.3 to 7.0	V
Output Clamp Voltage (4) 5.0 mA ≤ I_{OUT} ≤ 0.5 A	$V_{OUT(OFF)}$	 45 to 65	V
Output Self-Limit Current	$I_{OUT(LIM)}$	1.0 to 3.0	A
Continuous Per Output Current (4), (5)	$I_{OUT(CONT)}$	500	mA
ESD Voltage (6) Human Body Model (7) Machine Model (7)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Output Clamp Energy (8)	E_{CLAMP}	50	mJ
Recommended Frequency of SPI Operation	f_{SPI}	3.0	MHz
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Case Temperature	T_C	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Power Dissipation (T_A = 25°C) (9)	P_D	2.0	W
Peak Package Reflow Temperature During Reflow (10), (11)	T_{PPRT}	Note 11.	°C

Notes

1. Transient capability with external 100 Ω resistor in series with V_{PWR} pin and supply.
2. Exceeding these limits may cause a malfunction or permanent damage to the device.
3. Exceeding the limits on SCLK, SI, $\overline{CS}$, SFPD, or $\overline{RST}$ pins may cause permanent damage to the device.
4. With output OFF.
5. Continuous output current rating so long as maximum junction temperature is not exceeded. Operation at 125°C ambient temperature will require maximum output current computation using package $R_{\theta JA}$.
6. ESD data available upon request.
7. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 200 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200pF, R_{ZAP} = 0 Ω).
8. Maximum output clamp energy capability at 150°C junction temperature using a single non-repetitive pulse method.
9. Maximum power dissipation at indicated junction temperature with no heat sink used.
10. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
11. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

Table 3. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Thermal Resistance			°C/W
Junction-to-Ambient (Natural Convection, Single-Layer Board) (12), (13)	$R_{\theta JA}$	68	
Junction-to-Ambient (Natural Convection, Four-Layer Board) (12), (14)	$R_{\theta JMA}$	44	
Junction to Board (15)	$R_{\theta JL}$	20	

Notes

12. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
13. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
14. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
15. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate value with V_{BAT} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range					V
Quasi-Functional (16)	$V_{PWR(QF)}$	5.5	–	9.0	
Fully Operational	$V_{PWR(FO)}$	9.0	–	26.5	
Supply Current (All Outputs ON, I_{OUT} = 0.5 A)	$V_{PWR(ON)}$	–	1.0	2.0	mA
Sleep State Supply Current at $\overline{RST}$ ≤ 0.2 V_{DD} and/or V_{DD} < 0.5 V	$I_{PWR(ON)}$	–	1.0	2.5	µA
Sleep State Output Leakage Current (Per Output, $\overline{RST}$ = 0 V)	$I_{PWR(SS)}$	–	1.0	2.5	µA
Overvoltage Shutdown	V_{OV}	28	32	36	V
Overvoltage Shutdown Hysteresis (17)	$V_{OV(HYS)}$	0.2	0.8	1.5	V
Logic Supply Voltage	V_{DD}	4.5	–	5.5	V
Logic Supply Current (18)	I_{DD}				
$\overline{RST}$ ≥ 0.7 V_{DD}		–	1.0	4.0	mA
$\overline{RST}$ ≤ 0.5 V		–	–	25	µA
Logic Supply Undervoltage Lockout Threshold (19)	$V_{DD(UVLO)}$	2.5	–	3.5	V
POWER OUTPUT					
Drain-to-Source ON Resistance (I_{OUT} = 0.5 A, T_J - 25°C)	RDS(ON)				Ω
V_{PWR} = 5.5 V		–	–	2.0	
V_{PWR} = 9.0 V		–	0.6	1.2	
V_{PWR} = 13 V		–	0.55	1.0	
Drain-to-Source ON Resistance (I_{OUT} = 0.5 A, T_J - 150°C)	RDS(ON)				Ω
V_{PWR} = 5.5 V		–	–	3.0	
V_{PWR} = 9.0 V		–	1.2	1.6	
V_{PWR} = 13 V		–	1.0	1.2	
Output Self-Limiting Current	$I_{OUT(LIM)}$				A
Outputs Programmed ON, V_{OUT} = 0.6 V_{DD}		1.0	2.0	3.0	
Output Fault Detect Threshold (20)	$V_{OUTth(F)}$				V
Output Programmed OFF		2.5	3.0	3.5	

Notes

16. SPI inputs and outputs operational. Fault status reporting may not be fully operational within this voltage range. Outputs remain operational somewhat below this V_{PWR} range, but $R_{DS(ON)}$ will increase, causing power dissipation to increase. Outputs will re-establish their instructed state following a V_{PWR} interruption as long as V_{DD} remains non-interrupted.
17. This parameter is guaranteed by design, but it is not production tested.
18. Measured with the $\overline{RST}$ pin held at a logic high state. Outputs can be OFF or ON or in any combination thereof.
19. Device incorporates a power-ON reset function. For V_{DD} less than the Undervoltage Lockout Threshold voltage, all data registers are reset and all outputs are disabled.
20. Output Fault Detect Threshold with outputs programmed OFF. Output fault detect thresholds are the same for output opens and shorts.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate value with V_{BAT} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
Output OFF Open Load Detect Current [21] Output Programmed OFF, V_{OUT} = 0.6 V_{DD}	I_{OCO}	30	50	100	µA
Output Clamp Voltage 2.0 mA ≤ I_{OUT} ≤ 200 mA	V_{OK}	45	53	65	V
Output Leakage Current (V_{DD} ≤ 2.0 V) [22]	$I_{OUT(LKG)}$	-25	0	25	µA
Overtemperature Shutdown (Outputs OFF) [23]	T_{LIM}	155	180	–	°C
Overtemperature Shutdown Hysteresis [23]	$T_{LIM(HYS)}$	–	10	20	°C
DIGITAL INTERFACE					
Input Logic High Voltage [24]	V_{IH}	0.7	–	1.0	V_{DD}
Input Logic Low Voltage [24]	V_{IL}	0	–	0.2	V_{DD}
Input Logic Threshold Hysteresis (SCLK, $\overline{RST}$, and SFPD) [25]	$V_{I(HYS)}$	50	100	500	mV
SI Pull-Up Current (SI = 0 V)	I_{SI}	0	10	20	µA
$\overline{CS}$ Pull-Up Current ($\overline{CS}$ = 0 V)	I_{CS}	0	10	20	µA
SCLK Pull-Down Current (SCLK = 5.0 V)	I_{SCLK}	0	10	20	µA
$\overline{RST}$ Pull-Down Current ($\overline{RST}$ = 5.0 V)	$I_{\overline{RST}}$	5.0	25	50	µA
SFPD Pull-Down Current (SFPD = 5.0 V)	I_{SFPD}	5.0	10	25	µA
SO High-State Output Voltage ($I_{\overline{OH}}$ = 1.0 mA)	V_{SOH}	V_{DD} - 0.4 V	V_{DD} - 0.2 V	–	V
SO Low-State Output Voltage (I_{OL} = -1.6 mA)	V_{SOL}	–	0.2	0.4	V
SO Tri-State Leakage Current ($\overline{CS}$ = 0.7 VDD, 0 V ≤ V_{SO} ≤ V_{DD})	I_{SOT}	-10	0	10	µA
Input Capacitance (0 V ≤ V_{DD} ≤ 5.5 V) [26]	C_{IN}	–	–	12	pF
SO Tn-State Capacitance (0 V ≤ V_{DD} ≤ 5.5 V) [27]	C_{SOT}	–	–	20	pF

Notes

21. Output OFF Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded to be OFF.
22. Output leakage current measured with the output OFF and at 16 V.
23. This parameter is guaranteed by design, but it is not production tested.
24. Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, SCLK, $\overline{RST}$, and SFPD inputs.
25. Hysteresis is characterized, but it is not production tested.
26. Input capacitance of SI $\overline{CS}$, SCLK, $\overline{RST}$, and SFPD for 0 V ≤ V_{DD} ≤ 5.5 V. This parameter is guaranteed by design, but it is not production tested.
27. Tri-state capacitance of SO for 0 V ≤ V_{DD} ≤ 5.5 V. This parameter is guaranteed by design, but it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Rise Time (V_{PWR} = 13 V, R_L = 26 Ω) (28)	t_R	0.4	5.0	20	µs
Output Fall Time (V_{PWR} = 13 V, R_L = 26 Ω) (28)	t_F	0.4	5.0	20	µs
Output Turn-ON Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (29)	$t_{DLY(ON)}$	1.0	15	50	µs
Output Turn-OFF Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (30)	$t_{DLY(OFF)}$	1.0	15	50	µs
Output Short Fault Disable Report Delay (31) SFPD = 0.2 x V_{DD}	$t_{DLY(SF)}$	70	150	250	µs
Output OFF Fault Report Delay (32) SFPD = 0.2 x V_{DD}	$t_{DLY(OFF)}$	70	150	250	µs
DIGITAL INTERFACE TIMING					
Required Low State Duration for $\overline{RST}$ (V_{IL} < 0.2 V_{DD}) (33)	$t_{W(\overline{RST})}$	–	50	167	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)	t_{LEAD}	–	50	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required for Setup Time)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required for Setup Time)	$t_{SI(SU)}$	–	25	83	ns
Falling Edge of SCLK to SI (Required for Hold Time)	$t_{SI(HOLD)}$	–	25	83	ns
SO Rise Time (C_L = 200 pF)	$t_{R(SO)}$	–	25	50	ns
SO Fall Time (C_L = 200 pF)	$t_{F(SO)}$	–	25	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Rise Time (34)	$t_{R(SI)}$	–	–	50	ns
SI, $\overline{CS}$, SCLK, Incoming Signal Fall Time (34)	$t_{F(SI)}$	–	–	50	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (35)	$t_{SO(EN)}$	–	–	110	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (36)	$t_{SO(DIS)}$	–	–	110	ns
Time from Rising Edge of SCLK to SO Data Valid (37) 0.2 V_{DD} ≤ SO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	–	65	105	ns

Notes

28. Output Rise and Fall time respectively measured across a 26 Ω resistive load at 10% to 90% and 90% to 10% voltage points.
29. Output Turn-ON Delay time measured from 50% rising edge of $\overline{CS}$ to 90% of Output OFF voltage (V_{PWR}) with R_L = 26 Ω resistive load.
30. Output Turn-OFF Delay time measured from 50% rising edge of $\overline{CS}$ to 10% of Output OFF voltage (V_{PWR}) with R_L = 26 Ω resistive load.
31. Propagation time of Short Fault Disable Report measured from 50% rising edge of $\overline{CS}$ to 10% Output OFF voltage (V_{PWR}), V_{PWR} = 6.0 V and SFPD = 0.2 x V_{DD}.
32. Output OFF Fault Report Delay measured from 50% rising edge of $\overline{CS}$ to 10% rising edge of Output OFF voltage (V_{PWR}).
33. $\overline{RST}$ Low duration measured with outputs enabled and going to OFF or disabled condition.
34. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
35. Time required for output status data to be available for use at the SO pin.
36. Time required for output status data to be terminated at the SO pin.
37. Time required to obtain valid data out from SO following the rise of SCLK. See Figure 7, page 10.

TIMING DIAGRAM

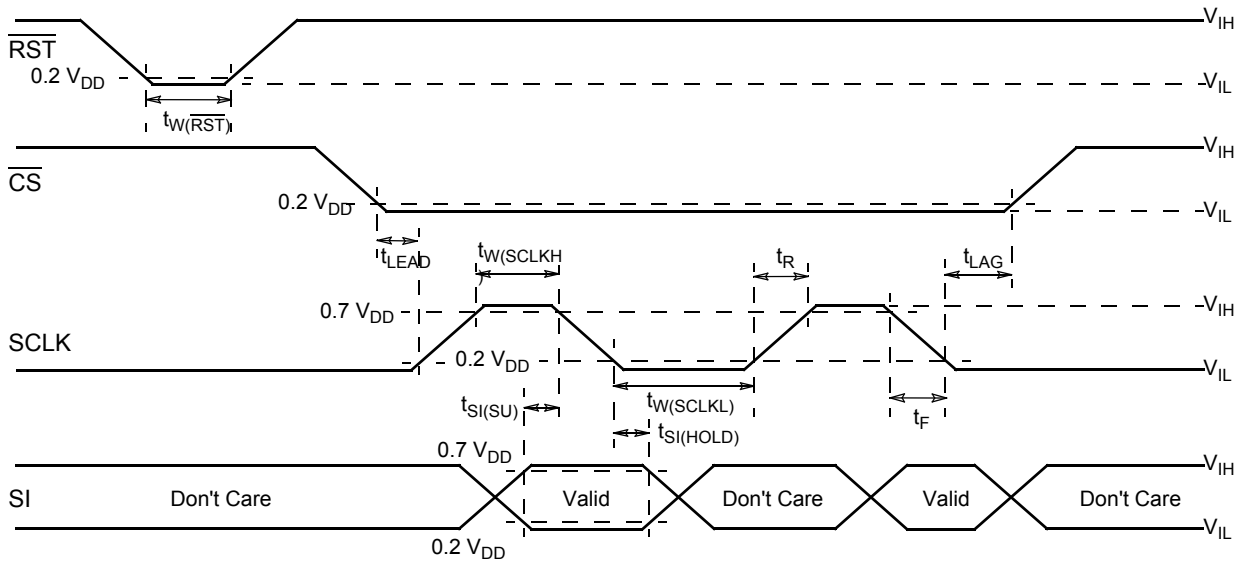
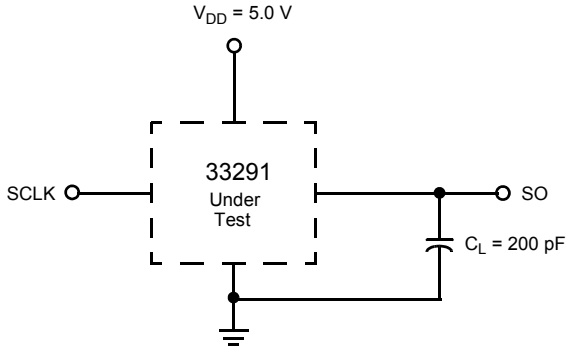


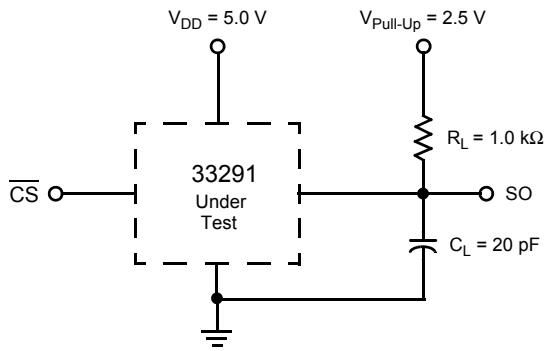
Figure 4. Input Timing Switch Characteristics

ELECTRICAL PERFORMANCE CURVES



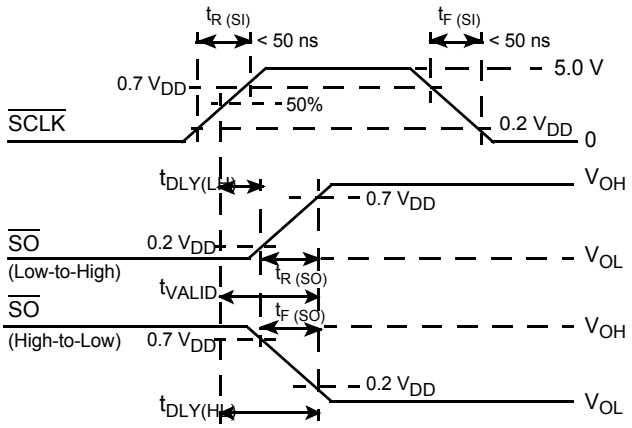
C_L represents the total capacitance of the test fixture and probe.

Figure 5. Valid Data Delay Time and Valid Time Test Circuit



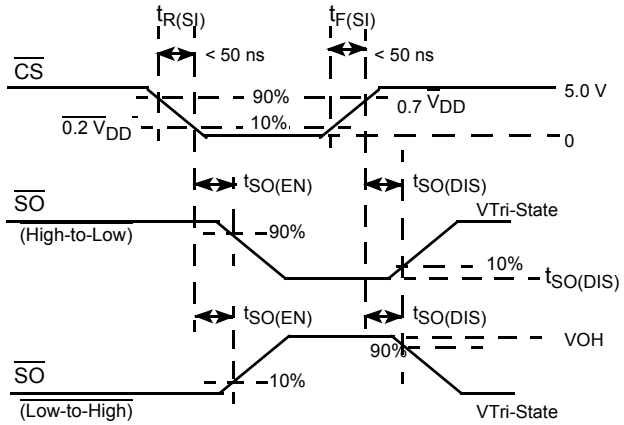
C_L represents the total capacitance of the test fixture and probe.

Figure 6. Enable and Disable Time Test Circuit



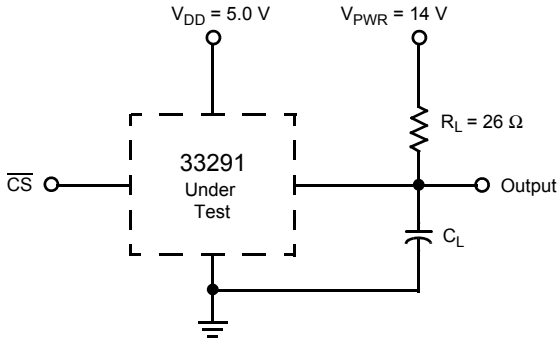
SO (Low-to-High) is for an output with internal conditions such that the low-to-high transition of $\overline{CS}$ causes the SO output to switch from high to low.

Figure 7. Valid Data Delay Time and Valid Time Waveforms



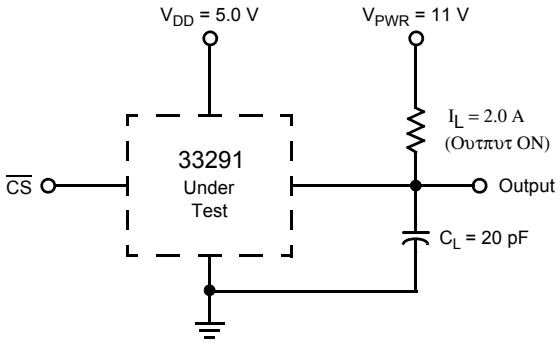
1. SO (high-to-low) waveform is for SO output with internal conditions such that SO output is low except when an output is disabled as a result of detecting a circuit fault with $\overline{CS}$ in a High Logic state; e.g., open load.
2. SO (low-to-high) waveform is for SO output with internal conditions such that SO output is high except when an output is disabled as a result of detecting a circuit fault with $\overline{CS}$ in a High Logic state; e.g., shortened load.

Figure 8. Enable and Disable Time Waveforms



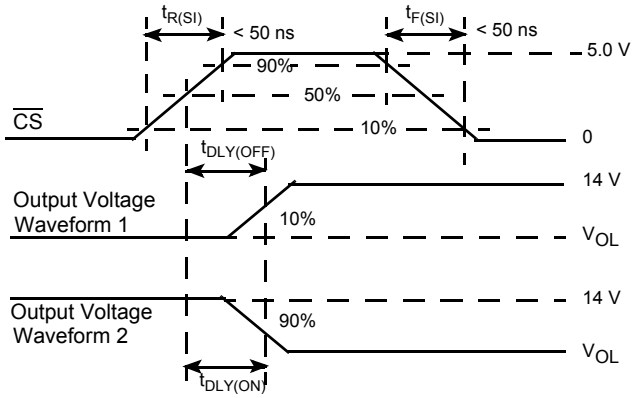
C_L represents the total capacitance of the test fixture and probe.

Figure 9. Switching Time Test Circuit



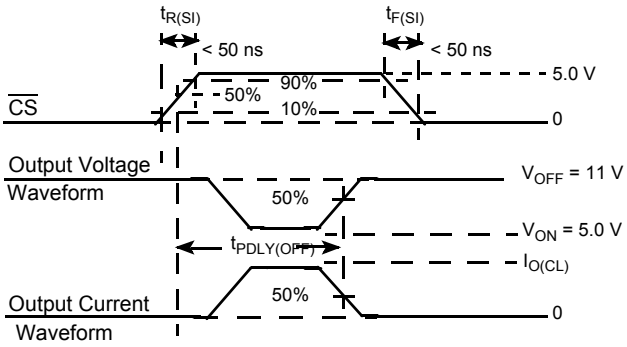
C_L represents the total capacitance of the test fixture and probe.

Figure 10. Output Fault Unlatch Disable Delay Test Circuit



1. $t_{DLY(ON)}$ and $t_{DLY(OFF)}$ are turn-ON and turn-OFF propagation delay times.
2. Turn-OFF is an output programmed from an ON to an OFF state.
3. Turn-ON is an output programmed from and OFF to an ON state.

Figure 11. Turn-On/-Off Waveforms



1. $t_{PDLY(OFF)}$ is the output fault unlatch disable propagation delay time required to correctly report an output fault after $\overline{CS}$ rises. It represents an output commanded ON while having an existing output short (overcurrent) to supply.
2. The SFPD pin $\leq$ 0.2 V.

Figure 12. Output Fault Unlatch Disable Delay Waveforms

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33291 was conceived, specified, designed, and developed for automotive applications. It is an eight-output low-side power switch having 8-bit serial control. The 33291 incorporates SMARTMOS technology having CMOS logic, bipolar/MOS analog circuitry, and independent state of the art double diffused MOS (DMOS) power output transistors. Many benefits are realized as a direct result of using this mixed technology. A simplified block diagram delineates 33291 in Figure 2.

Where bipolar devices require considerable control current for their operation, structured MOS devices, since they are voltage controlled, require only transient gate charging current affording a significant decrease in power consumption. The CMOS capability of the SMARTMOS process allows significant amounts of logic to be economically incorporated into the monolithic design. Additionally, the bipolar/MOS analog circuits embedded within the updrain power DMOS output transistors monitor and provide fast, independent protection control functions for each individual output. All outputs have internal 45 V at 0.5 A independent output voltage clamps to provide fast inductive turn-off and transient protection.

The 33291 uses high-efficiency updrain power DMOS output transistors exhibiting very low room temperature drain-to-source ON resistance values ($R_{DS(ON)} \leq 1.0\ \Omega$ at 13 V V_{PWR}) and dense CMOS control logic. Operational bias currents of less than 2.0 mA (1.0 mA typical) with any combination of outputs ON are the result of using this mixed technology and would not be possible with bipolar structures. To accomplish a comparable functional feature set using a bipolar structure approach would result in a device requiring hundreds of milliamperes of internal bias and control current. This would represent a very large amount of power to be consumed by the device itself and not available for load use.

During operation, the 33291 functions as an eight output serial switch serving as a microcontroller (MCU) bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions. The 33291 directly relieves the MCU of the fault management functions. The 33291 directly interfaces to an MCU, operating at system clock serial frequencies in excess of 3.0 MHz. It uses a Synchronous Peripheral Interface (SPI) for control and diagnostic readout. Figure 13 illustrates the basic SPI configuration between an MCU and one 33291.

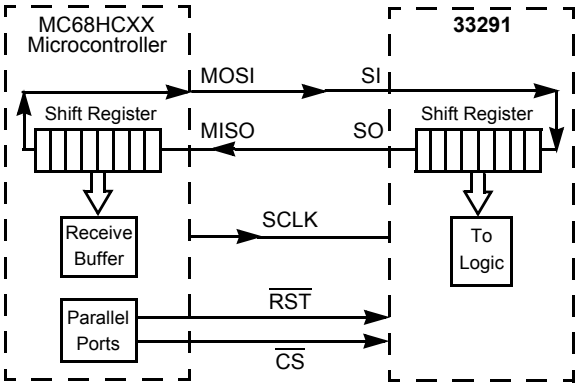


Figure 13. SPI Interface with Microcontroller

The circuit can also be used in a variety of other applications in the computer, telecommunications, and industrial fields. It is parametrically specified over an input battery/supply range of 9.0 V to 16 V but is designed to operate over a considerably wider range of 5.5 V to 26.5 V. The design incorporates the use of logic level MOSFETs as output devices. These MOSFETs are sufficiently turned ON with a gate voltage of less than 5.0 V, thus eliminating the need for an internal charge pump. Each output is identically sized and independent in operation. The efficiency of each output transistor is such that at room temperature with as little as 9.0 V supply (V_{PWR}), the maximum $R_{DS(ON)}$ of an output at room temperature is 1.2 Ω (0.9 Ω typical) and increases to only 2.0 Ω as V_{PWR} is decreased to 5.5 V.

All inputs are compatible with 5.0 V CMOS logic levels, incorporating negative or inverted logic. Whenever an input is programmed to a logic low state (<1.0 V) the corresponding low side switched output being controlled will be active low and turned ON. Conversely, whenever an input is programmed to a logic high state (>3.0 V), the output being controlled will be high and turned OFF.

One main advantage of the 33291 is the serial port. When coupled to an MCU, it receives ON/OFF commands from the MCU and in return transmits the drain status of the device's output switches. Many devices can be daisy-chained together, forming a larger system, as illustrated in Figure 14, page 13.

Note In this example, only one dedicated MCU parallel port (aside from the required SPI) is required for chip select to control 32 possible loads.

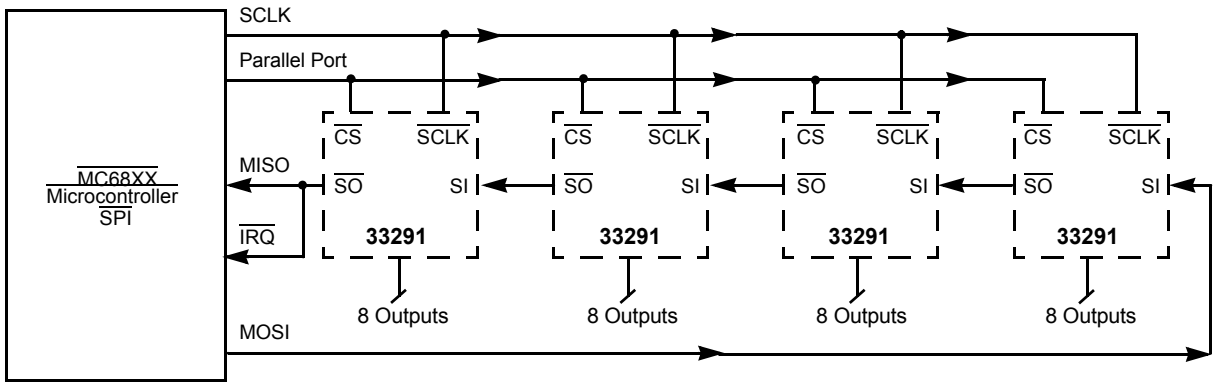


Figure 14. 33291 SPI System Daisy Chain

Multiple 33291 devices can also be controlled in a parallel input fashion using SPI, illustrated in Figure 15. This figure shows a possible 24 loads being controlled by only three dedicated parallel MCU ports used for chip select.

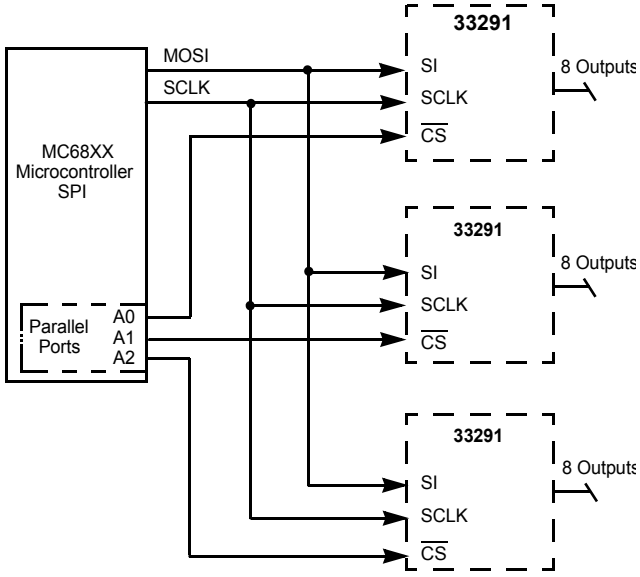


Figure 15. Parallel Input SPI Control

Figure 16, page 14, illustrates a basic method of controlling multiple 33291 devices using two MCUs. A system can have only one master MCU at any given instant of time and one or more slave MCUs. Master control of the system must pass from one MCU to the other in an orderly manner. The master MCU supplies the system clock signal (top MCU designated the master); the lower MCU being the slave. It is possible to have a system with more than one master; however, not at the same time. Only when the master is not communicating can a slave assume the *mastership* and communicate. MCU master control is switched through the use of the slave select ($\overline{SS}$) pin of the MCUs. A master will become a slave when it detects a logic low state on its $\overline{SS}$ pin.

These basic examples make the 33291 very attractive for applications where a large number of loads require efficient control. To this end, the popular Synchronous Serial Peripheral Interface (SPI) protocol is incorporated to communicate efficiently with the MCU.

SPI SYSTEM ATTRIBUTES

The SPI system is flexible enough to communicate directly with numerous standard peripherals and MCUs available from Motorola and other semiconductor manufacturers. SPI reduces the number of pins necessary for input/output (I/O) on the 33291. It also offers an easy means of expanding the I/O function using few MCU pins. The SPI system of communication consists of the MCU transmitting, in return it receives one data-bit of information per system clock cycle.

Data bits of information are simultaneously transmitted by one pin, Master Out Serial In (MOSI), and received by another pin, Master In Serial Out (MISO), of the MCU.

Some features of SPI are as follows:

- Full duplex, three-wire synchronous data transfer
- Each microcontroller can be a master or a slave
- Provides write collision flag protection
- Provides end of message interrupt flag
- Four I/Os associated with SPI (MOSI, MISO, SCLK, SS)
- Drawbacks to SPI are as follows:
- An MCU is required for efficient operational control
- In contrast to parallel input control it is slower at performing pulse width modulating (PWM) functions.

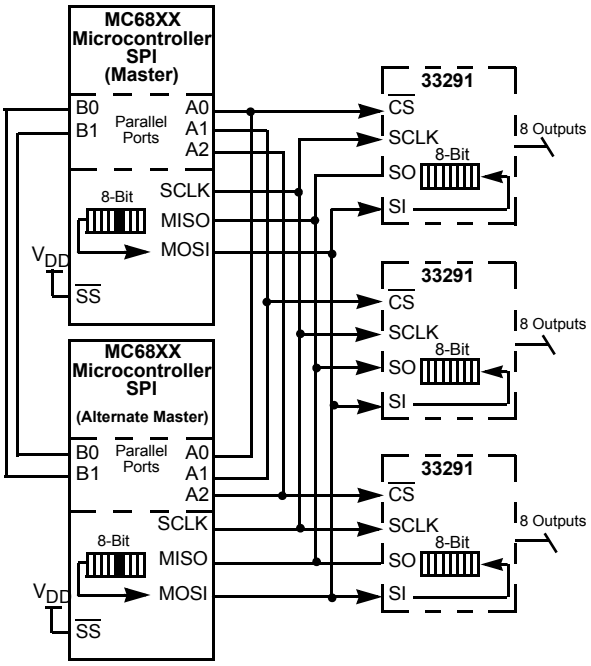


Figure 16. Multiple MCU SPI Control

FUNCTIONAL PIN DESCRIPTION

CHIP SELECT ($\overline{CS}$)

The 33291 receives its MCU communication through the $\overline{CS}$ pin. Whenever this pin is in a logic low state, data can be transferred from the MCU to the 33291 by way of the SI pin and from the 33291 to the MCU through the SO pin. Clocked-in data from the MCU is transferred from the 33291 Shift register and latched into the power outputs on the rising edge of the $\overline{CS}$ signal. On the falling edge of the $\overline{CS}$ signal, drain status information is transferred from the power outputs then loaded into the Shift register of the device. The $\overline{CS}$ pin also controls the output driver of the serial output (SO) pin. Whenever the $\overline{CS}$ pin goes to a logic low state, the SO pin output driver is enabled allowing information to be transferred from the 33291 to the MCU. To avoid data corruption or the generation of spurious data, it is essential the high-to-low transition of the $\overline{CS}$ signal occur only when SCLK is in a logic low state.

SYSTEM CLOCK (SCLK)

The system clock (SCLK) pin clocks the internal shift registers of the 33291. The serial input (SI) pin accepts data into the Input Shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. False clocking of the Shift register must be avoided to guarantee validity of data. It is essential the SCLK pin be in a logic low state whenever the chip select bar ($\overline{CS}$) pin makes any transition. For this reason, it is recommended, though not absolutely necessary, the SCLK pin be kept in a low logic state as long as the device is not accessed ($\overline{CS}$ in logic high state). When $\overline{CS}$ is in a logic high state, signals at the SCLK and SI pins are ignored and SO is tri-stated (high impedance). See the Data Transfer Timing diagram in Figure 18, page 17.

SERIAL INSTRUCTION (SI)

This pin is for the input of serial instruction (SI) data. SI is read on the falling edge of SCLK. A logic high state present on this pin when the SCLK signal rises will program a specific output OFF. In turn, $\overline{CS}$ pin turns OFF the specific output on the rising edge of the $\overline{CS}$ signal. Conversely, a logic low state present on the SI pin will program the output ON, In turn, the pin turns ON the specific output on the rising edge of the $\overline{CS}$ signal.

To program the eight outputs of the 33291 ON or OFF, an 8-bit serial stream of data is required to be synchronously entered into the SI pin starting with Output 7, followed by Output 6, Output 5, and so on, to Output 0. Referring to Figure 18, the DO bit is the most significant bit (MSB) corresponding to Output 7. For each rise of the SCLK signal, with $\overline{CS}$ held in a logic low state, a data-bit instruction (ON or OFF) is synchronously loaded into the Shift register per the data-bit SI state. The Shift register is full after eight bits of information have been entered. To preserve data integrity, care should be taken to not transition SI as SCLK transitions from a low-to-high logic state.

SERIAL OUTPUT (SO)

The serial output (SO) pin is the tri-stateable output from the Shift register. The SO pin remains in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. The SO data reports the drain status, either high or low relative to the previous command word. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. When an output is OFF and not faulted, the corresponding SO data-bit is a high state. When an output is ON, and there is no fault, the corresponding data-bit on the SO pin will be a low logic state. The SI/SO shifting of data follows a first-in-first-out (FIFO) protocol with both input and output words transferring the MSB first. Referring to Figure 18, the DO bit is the MSB corresponding to Output 7 relative to the previous command word. The SO pin is not affected by the status of the $\overline{RST}$ pin.

RESET ($\overline{RST}$)

The 33291 Reset ($\overline{RST}$) pin is active low. It is used to clear the SPI Shift register. In doing so, all output switches are set at OFF. With the device in a system with an MCU, upon initial system power-up, the MCU holds the $\overline{RST}$ pin of the device in a logic low state, ensuring all outputs to be OFF until both the V_{DD} and V_{PWR} pin voltages are adequate for predictable operation. After the 33291 is reset, the MCU is ready to assert system control with all output switches initially OFF.

If the V_{PWR} pin of the 33291 experiences a low voltage, following normal operation, the MCU should pull the $\overline{RST}$ pin low to shut down the outputs and clear the input data register. The $\overline{RST}$ pin is active low and has an internal pull-down incorporated to ensure operational predictability should the external pull-down of the MCU open circuit. The internal pull-down is only 25 μA, affording safe and easy interfacing to the MCU. The $\overline{RST}$ pin of the 33291 should be pulled to a logic low state for a duration of at least 250 ns to ensure reliable a reset.

A simple power ON reset delay of the system can be programmed through the use of an RC network comprised of a shunt capacitor from the $\overline{RST}$ pin to Ground and a resistor to V_{DD}, illustrated in Figure 17. Care should be exercised ensuring proper discharge of the capacitor. Careful attention eliminates adverse delay of the $\overline{RST}$ and damage of the MCU if it pulls the Reset line low, thereby accomplishing initialization for turn ON delay. It may be easier to incorporate delay into the software program and use a parallel port pin of the MCU to control the 33291 $\overline{RST}$ pin.

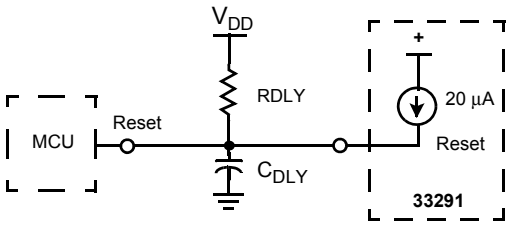


Figure 17. Power ON Reset

SHORT FAULT PROTECT DISABLE (SFPD)

The Short Fault Protect Disable (SFPD) pin is used to prevent the outputs from latching-off due to an overcurrent condition. This feature provides control of incandescent lamp loads where in-rush currents exceed the device's analog current limits. Essentially the SFPD pin determines whether the 33291 output(s) will instantly shut down upon sensing an output short or remain ON in a current limiting mode of operation until the output short is removed or thermal shutdown is reached. If the SFPD pin is tied to V_{DD} = 5.0 V the 33291 output(s) will remain ON in a current limited mode of operation upon encountering a load short to supply or overcurrent condition. When the SFPD pin is grounded, a short circuit will immediately shut down only the output affected. Other outputs not having a fault condition will operate normally. The short circuit operation is addressed in more detail later.

POWER CONSUMPTION

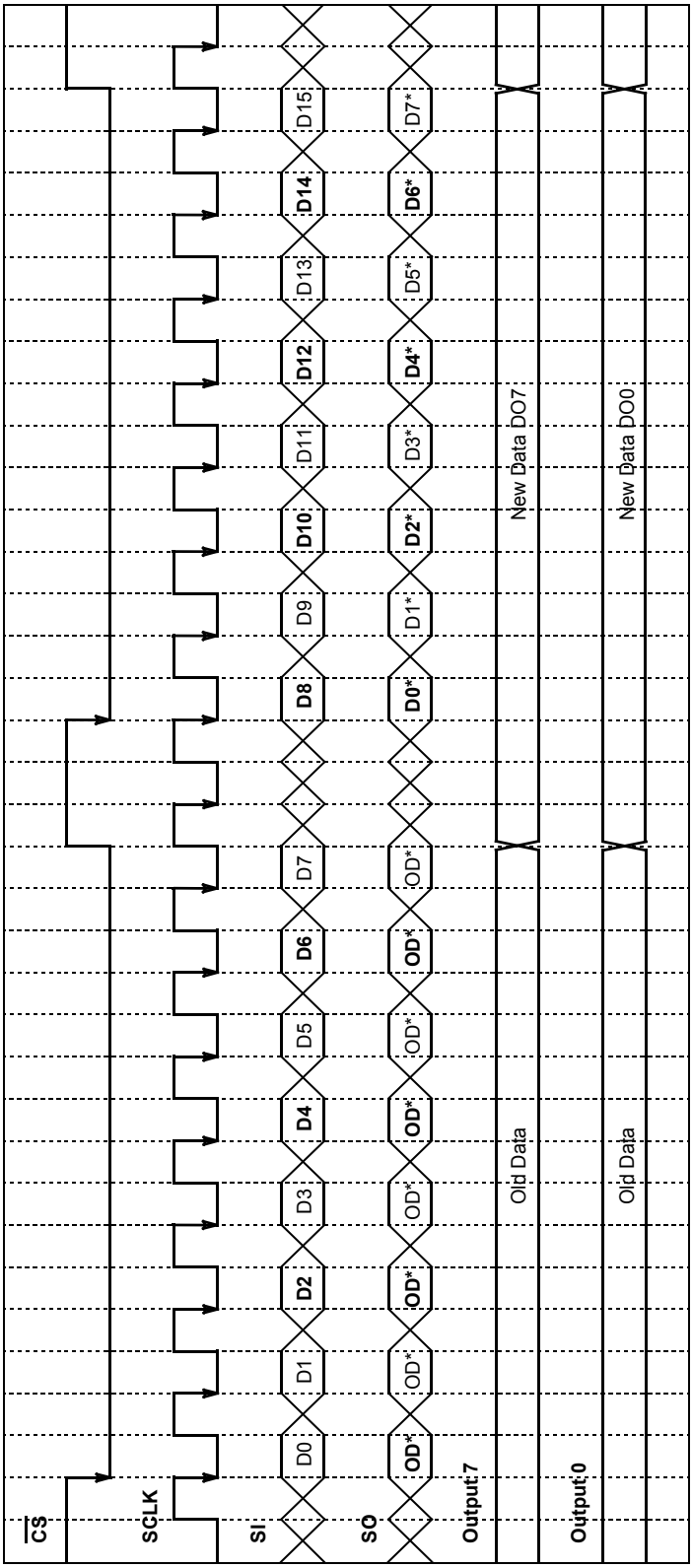
The 33291 has extremely low power consumption in both the operating and standby modes. In the standby, or *Sleep,* mode, with $V_{DD} \leq 2.0$ V, the current consumed by the VPWR pin is less than 25 µA. In the operating mode, the current drawn by the VDD pin is less than 4.0 mA (1.0 mA typical) while the current drawn at the VPWR pin is 2.0 mA maximum (1.0 mA typical). During normal operation, turning outputs ON increases I_{PWR} by only 20 µA per output. Each output experiencing a *soft short* (overcurrent conditions just under the current limit) adds 0.5 mA to the I_{PWR} current

PARALLELING OF OUTPUTS

Using MOSFETs as output switches permits connecting any combination of outputs together. $R_{DS(ON)}$ of MOSFETs have an inherent positive temperature coefficient providing balanced current sharing between outputs without destructive operation (bipolar outputs could not be paralleled in this fashion as thermal run-away would likely occur). The device can even be operated with all outputs tied together. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents.

Performance of parallel operation results in a corresponding decrease in $R_{DS(ON)}$ while the Output OFF Open Load Detect Currents and the Output Current Limits increase correspondingly (by a factor of eight if all outputs are paralleled). Less than 125 mΩ $R_{DS(ON)}$ at 25°C with current limiting of 8 A to 24 A will result if all outputs are paralleled together. There will be no change in the overvoltage detect or the OFF output threshold voltage range. The advantage of paralleling outputs within the same 33291 affords the existence of minimal $R_{DS(ON)}$ and output clamp voltage variation between outputs.

Typically, the variation of $R_{DS(ON)}$ between outputs of the same device is less than 0.5 percent. The variation in clamp voltages, potentially affecting dynamic current sharing, is less than five percent. Paralleling outputs from two or more different devices is possible, but it is not recommended. There is no guarantee the $R_{DS(ON)}$ and clamp voltage of the two devices will match. System level thermal design analysis and verification should be conducted whenever paralleling outputs, particularly where different devices are involved.



NOTES: 1.$\overline{RST}$ pin is in a logic high-state during the above operation.
2.D0, D1, D2, ..., and D15 relate to the ordered entry of program data into the MC33291 with D0/D8 bits (MSB) corresponding to Output 7 and D7/D15 corresponding to Output 0.
3.D0*, D1*, D2*, ..., and D7* relate to the ordered data out of the MC33291 with D0* bit (MSB) corresponding to Output 7.
4.OD* corresponds to Old Databits.
5.For brevity, only DO7 and DO0 are shown which respectively correspond to Output 7 and Output 0.

Figure 18. Data Transfer Timing

Data Transfer Timing (General)

$\overline{CS}$ High-to-Low	SO pin is enabled. Output Status information transferred to Output Shift Register.
$\overline{CS}$ Low-to-High	Data from the Shift Register is transferred to the Output Power Switches.
SO	Will change state on the rising edge of the SCLK pin signal.
SI	Will accept data on the falling edge of the SCLK pin signal.

FAULT LOGIC OPERATION

INTRODUCTION

The MCU can perform a parity check of the fault logic operation by comparing the command 8-bit word to the status 8-bit word. Assume after system reset, the MCU first sends an 8-bit command word to the 33291. This word is called Command Word 1. Each output to be turned ON will have its corresponding data bit low. Refer to the data transfer timing illustration in Figure 18.

As Command Word 1 is being written into the Shift register of the 33291, a status word is being simultaneously written and received by the MCU. However, the word being received by the MCU is the status of the previous write word to the 33291, Status Word 0. If the command word of the MCU is written a second time (Command Word 2 = Command Word 1), the word received by the MCU, Status Word 2, is the status of Command Word 1. The timing diagram illustrated in Figure 18 depicts this operation. Status Word 2 is then compared with Command Word 1. The MCU will Exclusive OR Status Word 2 with Command Word 1 to determine if the two words are identical. If the two words are identical, no faults exist. The timing between the two write words must be greater than 100 μs to receive proper drain status. The system data bus integrity may be tested by writing two like words to the 33291 within a few microseconds of each other.

INITIAL SYSTEM SETUP TIMING

The MCU can monitor two kinds of faults:

1. Communication errors on the data bus
2. Actual faults of the output loads

After initial system startup or reset, the MCU will write one word to the 33291. If the word is repeated within approximately five microseconds of the first word, the word received by the MCU, at the end of the repeated word, serves as a confirmation of data bus integrity (1). At startup, the 33291 will take 25 μs to 100 μs before a repeat of the first word should be repeated at least 100 μs later to verify the status of the outputs.

The SO of the 33291 will indicate any one of four faults. The four possible faults are:

1. Overtemperature
2. Output OFF Open Fault
3. Short Fault (overcurrent)
4. V_{PWR} Overvoltage Fault

With the exception of the Overvoltage Fault, all of these faults are output specific. Overtemperature Detect, Output OFF Open Detect, and Output Short Detect are dedicated to each output separately such that the outputs are independent in operation. A V_{PWR} Overvoltage Detect is of a *global* nature, causing all outputs to be turned OFF.

OVERTEMPERATURE FAULT

Patent pending Overtemperature Detect and shutdown circuits are specifically incorporated for each individual output. The shutdown following an Overtemperature condition is independent of the system clock or any other logic signal. Each independent output shuts down at 155°C to 185°C. When an output shuts down due to an Overtemperature Fault, no other outputs are affected. The MCU recognizes the fault since the output was commanded to be ON and the status word indicates it is OFF. A maximum hysteresis of 20°C ensures an adequate time delay between output turn OFF and recovery. This avoids a very rapid turn ON and turn OFF of the device around the Overtemperature threshold. When the temperature falls below the recovery level for the Overtemperature Fault, the device will turn ON only if the Command Word during the next write cycle indicates the output should be turned ON.

OVERVOLTAGE FAULT

An Overvoltage condition on the VPWR pin causes the 33291 to shut down all outputs until the overvoltage condition is removed and the device is re-programmed by the SPI. The overvoltage threshold on the VPWR pin is specified as 28 V to 36 V with 1.0 V typical hysteresis. Following the overvoltage condition, the next write cycle sends the SO pin the hexadecimal word $FF (all ones), indicating all outputs are turned OFF. In this way, potentially dangerous timing problems are avoided and the MCU reset routine ensures an orderly startup of the loads. The 33291 does not detect an overvoltage on the VDD pin. Other external circuitry, such as the Freescale 33161 Universal Voltage Monitor, is necessary to accomplish this function.

OUTPUT OFF OPEN LOAD FAULT

An Output OFF Open Load Fault is the detection and reporting of an *open* load when the corresponding output is disabled (input bit programmed to a logic high state). To understand the operation of the Open Load Fault detect circuit, see Figure 19. The Output OFF Open Load Fault is detected by comparing the drain voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

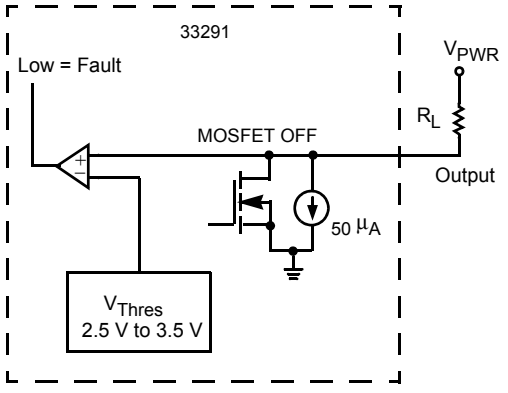


Figure 19. Output OFF Open Load Fault

An Output OFF Open Load Fault is indicates when the output voltage is less than the Output Threshold Voltage (V_{THRES}) of 0.6 to 0.8 x V_{DD}. Since the 33291 outputs function as switches, during normal operation, each MOSFET output should either be completely turned ON or OFF. By design, the threshold voltage was selected to be between the ON and OFF voltage of the MOSFET. During normal operation, the ON state V_{DS} voltage of the MOSFET is less than the threshold voltage and the OFF state V_{DS} voltage is greater than the threshold voltage. This design approach affords using the same threshold comparator for Output Open Load Detect in the OFF state and Short Circuit Detect in the ON state. (See Figure 20 for an understanding of the Short Circuit Detect circuit.) With V_{DD} = 5.0 V, an OFF state output voltage of less than 3.0 V will be detected as an Output OFF Open Load Fault while voltages greater than 4.0 V will not be detected as a fault.

The 33291 has an internal pull-down current source of 50 μA, illustrated in Figure 19, page 18, between the MOSFET drain and ground. This current source prevents the output from floating up to V_{PWR} if there is an open load or internal wire bond failure. The internal comparator compares the drain voltage with a reference voltage, V_{THRES} (0.6 to 0.8 x V_{DD}). If the output voltage is less than this reference voltage, the 33291 will declare the condition to be an open load fault.

During output switching, especially with capacitive loads, a false output OFF Open Load Fault may be triggered. To prevent this false fault from being reported, an internal fault filter in the range of 25 μs to 100 μs is incorporated. The duration in which a false fault may be reported is a function of the load impedance (R_L,C_L,L_L), $R_{DS(ON)}$, and C_{OUT} of the MOSFET as well as the supply voltage (V_{PWR}). The rising edge of $\overline{CS}$ triggers a built-in fault delay timer which must time out (25 μs or 100 μs) before the fault comparator is enabled to detect at faulted threshold. The circuit automatically returns to normal operation once the condition causing the Open Load Fault is removed.

SHORTED LOAD FAULT

A short load, or overcurrent fault can be caused by any output being shorted directly to supply, or an output experiencing a current greater than the current limit.

There are three safety circuits progressively in operation during load short conditions providing system protection. They are as follows:

1. The output current of the device is monitored in an analog fashion using a SENSEFET approach and current limited.
2. The output current of the device is sensed by monitoring the MOSFET drain voltage.
3. The output thermal limit of the device is sensed and when attained causes only the specific faulted output to be latched OFF, allowing all remaining outputs to operate normally.

All three protection mechanisms are incorporated in their output, affording robust independent output operation.

The analog current limit circuit is always active and monitors the output drain current. An overcurrent condition causes the gate control circuitry to reduce the gate-to-source voltage imposed on the output MOSFET, re-establishing the load current in compliance with current limit (1.0 A to 3.0 A) range. The time required for the current limit circuitry to act is less than 20 μs. Therefore, currents higher than 1.0 A to 3.0 A will never be seen for more than 20 μs (a typical duration is 10 μs). If the current of an output attempts to exceed the predetermined limit of 1.0 A to 3.0 A (2.0 A nominal), the V_{DS} voltage will exceed the V_{THRES} voltage and the overcurrent comparator will be tripped as shown in Figure 20.

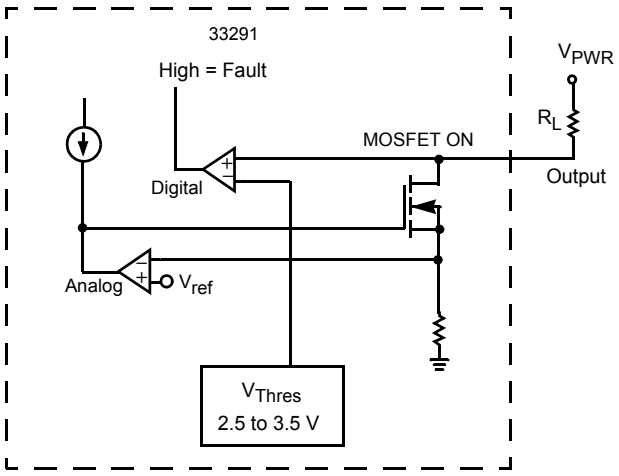


Figure 20. Short Circuit Detect and Analog Current Limiting Circuit

The status of SFPD determines whether the 33291 will shut down immediately or continue to operate in an analog current limited mode until either the short circuit (overcurrent) condition is removed or thermal shutdown is reached.

Grounding the SFPD pin will enable the short fault protection shutdown circuitry. Consider a load short (output short to supply) occurring on an output before, during, and after output turn ON. When the $\overline{CS}$ signal rises to the high logic state, the corresponding output is turned ON and a delay timer is activated. The duration of the delay timer is 70 μs to 250 μs. If the short circuit takes place before the output is turned ON, the delay experienced is the entire 70 μs to 250 μs followed by shutdown. If the short occurs during the delay time, the shutdown still occurs after the delay time has elapsed. However, if the short circuit occurs after the delay time, shutdown is immediate (within 20 μs after sensing). The purpose of the delay timer is to prevent false faults from being reported when switching capacitive loads.

If the SFPD pin is at 5.0 V (or V_{DD}), an output will not be disabled when an overcurrent is detected. The specific output will, within 5.0 μs to 10 μs of encountering the short circuit, go into an analog current limited mode. This feature is especially

useful when switching incandescent lamp loads, where high in-rush currents experienced during startup last for 10 ms to 20 ms.

Each output of the 33291 has its own overcurrent shutdown circuitry. Overtemperature faults and overvoltage faults are not affected by the SFPD pin's state.

Both load current sensing and output voltage sensing are incorporated for Short Fault detection with actual detection occurring slightly after the onset of current limit. The current limit circuitry incorporates a SENSEFET approach to measure the total drain current. This calls for the current through a small number of cells in the power MOSFET to be measured and the result multiplied by a constant, giving the total current. Whereas an output shutdown circuitry measures the drain-to-source voltage, shutting down the output if its threshold (V_{THRES}) will be exceeded.

Short fault detection is accomplished by sensing the output voltage and comparing it to V_{Thres}. The lowest V_{THRES} requires a voltage of 2.5 V to be sensed. For an enabled output, with V_{DD} = 5.0 ± 0.5 V, an output voltage in excess of 3.5 V will be detected as a short (overcurrent condition), while voltages less than 2.5 V will not be detected as shorts.

OVERCURRENT RECOVERY

If the SFPD pin is in a high logic state, the circuit returns to normal operation automatically after the short circuit is removed (unless thermal shutdown has occurred).

If the SFPD pin is grounded and overcurrent shutdown occurs, removing the short circuit will result in the output remaining OFF until the next write cycle. If the short circuit is not removed, the output will turn ON for the delay time (70 μs to 250 μs) and then turn OFF for every write cycle commanding a turn ON.

SFPD PIN VOLTAGE SELECTION

Since the voltage condition of the SFPD pin controls the activation of the short fault protection (i.e., shutdown) mode equally for all eight outputs, the load having the longest duration of in-rush current determines what voltage (state) the SFPD pin should be. Usually if at least one load is, say an incandescent lamp, the in-rush current on that input will be milliseconds in duration. Therefore, setting SFPD at 5.0 V will prevent shutdown of the output due to the in-rush current. The system relies only on the overtemperature shutdown to protect the outputs and the loads. The 33291 was designed to switch GE194 incandescent lamps (or equivalents) with the SFPD pin in a grounded state. Considerably larger lamps can be switched with the SFPD pin held in a high logic state.

Sometimes both a delay period greater than 70 μs to 250 μs (current limiting of the output) followed by an immediate overcurrent shutdown is necessary. This can be accomplished by programming the SFPD pin to 5.0 V for the extended delay period, allowing the outputs to remain ON in a current limited mode, then grounding it to accomplish the immediate shutdown after a period of time. Additional external circuitry is required to implement this type of function. An MCU parallel output port can be devoted to controlling the SFPD voltage during and after the delay period; this is often a much better method. In either case, care should be taken to execute the SFPD start-up routine every time startup or reset occurs.

UNDERVOLTAGE SHUTDOWN

An undervoltage V_{DD} condition will result in the global shutdown of all outputs. The undervoltage threshold is between 2.5 V and 3.5 V. When V_{DD} goes below the threshold, all outputs are turned OFF and the Serial Output data register is reset to indicate the same.

An undervoltage condition at the VPWR pin will not cause output shutdown and reset. When V_{PWR} is between 5.5 V and 9.0 V, the outputs will operate per the command word. However, the status as reported by the SO pin may not be accurate below 9.0 V V_{PWR}. Proper operation at V_{PWR} voltages below 5.5 V are not be guaranteed.

DECIPHERING FAULT TYPE

The 33291 SO pin can be used to determine what kind of system fault has occurred. With eight outputs having open load, overcurrent, overtemperature, and overvoltage faults, a total of 25 different faults are possible. The SO status word received by the MCU will be compared with the word sent to the 33291 during the previous write cycle. For a specific output, if the SO bit compares with the corresponding SI bit of the previous word, the output is operating normal with no fault. Only when the SO bit and previous word SI bit differ is there a fault indicated. If the two words are not the same, the MCU should be programmed to determine which output or outputs are faulted.

If for a specific output the initial SI command bit were logic high, the output would be programmed to be *off*; if upon the next command word being entered, a logic low came back on SO, for that specific output's corresponding bit an *output-off open-load* fault would be indicated. The resulting SO bit for that specific output would be different from that entered during the previous word for that SI bit, indicating the fault. The eight output-off open-load faults are therefore most easily detected.

If for a specific output the initial SI command bit were a logic low, when calling for the output to be programmed *on*, the next word command entered into the corresponding bit returns with a logic high on SO. An output overcurrent fault would be indicated. An overcurrent fault is always reported by the SO output and is independent of the logic state existing on the SFPD pin. When the SFPD pin is in a logic high state, an overcurrent condition will be reported on the SO pin. However, limiting output current is in effect and the output is permitted to operate if the overcurrent condition does not drive output into an overtemperature fault. An overtemperature fault will shut down the specific output effected for the duration of the overtemperature condition.

Overcurrent and overtemperature faults are often related. Turning the effected output switches OFF and waiting for some time to allow the output to cool down should make these types of faults go away. *Soft* overcurrent faults can

sometimes be determined over hard short faults and overtemperature faults by observing the time required for the device to recover. However, in general overcurrent and overtemperature faults cannot be differentiated in normal application usage.

An advantage of the synchronous serial output is multiple faults can be detected with only one (SO) pin being used for fault status reporting.

If V_{PWR} experiences an overvoltage condition, all outputs will immediately be turned OFF and remain latched OFF. A new command word is required to turn the outputs back ON following an overvoltage condition.

Output Voltage Clamping

Each output of the 33291 incorporates an internal voltage clamp to provide fast turn-off and transient protection of the output. Each clamp independently limits the drain-to-source voltage to 53 V at drain currents of 0.5 A and keeps the output transistors from avalanching by causing the transient energy to be dissipated in the linear mode (see Figure 21). The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) times the duration the clamp is active (t).

Characterization of the output clamps, using a single pulse non-repetitive method at 0.5 A, indicates the maximum energy to be 50 mJ at 150°C junction temperature per output.

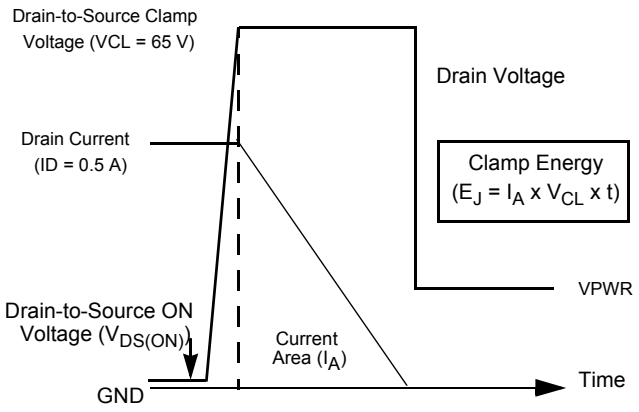


Figure 21. Output Voltage Clamping

THERMAL CHARACTERIZATION

THERMAL MODEL

Logic functions take up a very small area of the die and generate negligible power. In contrast, the output transistors take up most of the die area and are the primary contributors of power generation. The thermal model illustrated in Figure 22, page 22, was developed for the 33291 mounted on a typical PC board. The model is accurate for both steady state and transient thermal conditions. The components R_{d0} through R_{d7} represent the steady state thermal resistance of the silicon die for transistor outputs 0 through 7, while C_{d0} through C_{d7} represent the corresponding thermal capacitance of the silicone die translator outputs and plastic. The device area and die thickness determine the values of these specific components.

The thermal impedance of the package from the internal mounting flag to the outside environment is represented by the terms R_{PKG} and C_{PKG}. The steady state thermal resistance of leads and the PC board make up the steady state package thermal resistance, R_{pkg}. The thermal capacitance of the package is made up of the combined capacitance of the flag and the PC board. The mode compound was not modeled as a specific component but it is factored into the other overall component values.

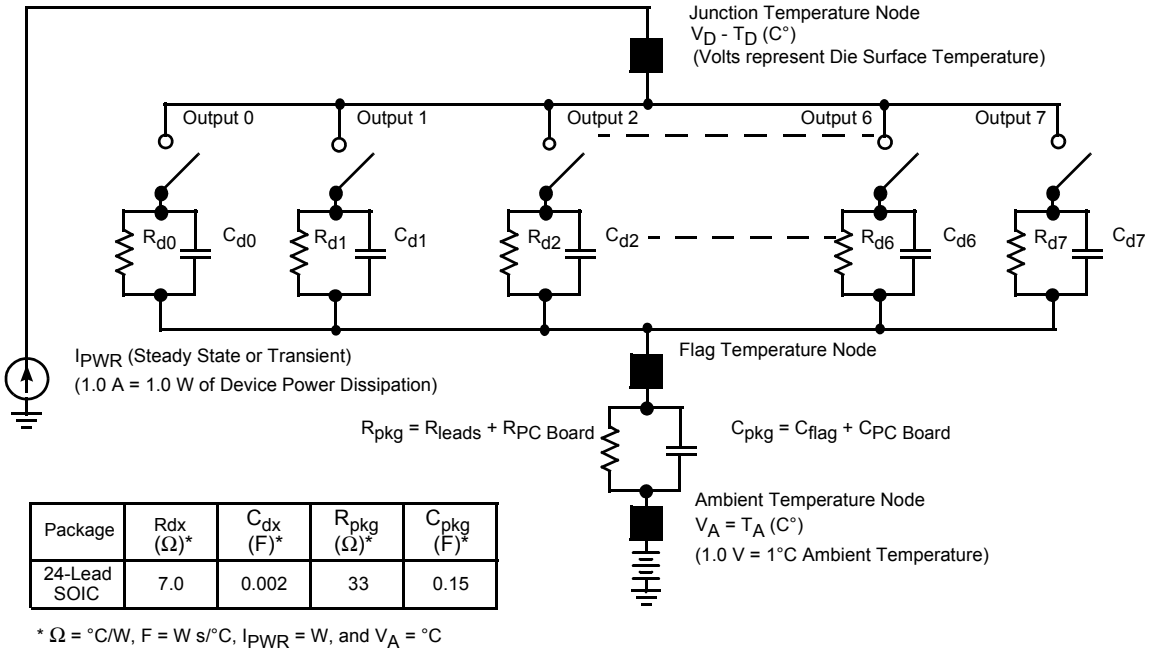
The battery voltage in the thermal model represents the ambient temperature the device and PC board are subjected to. The I_{PWR} current source represents the total power dissipation and is calculated by totalling the power dissipation of each individual output transistor. This is easily accomplished by knowing $R_{DS(ON)}$ and load current of the individual outputs.

Very satisfactory steady state and transient results are experienced with this thermal model. Tests indicate the model accuracy to have less than 10 percent error. Output interaction with an adjacent output is believed to be the main contributor to the thermal inaccuracy. Tests indicate little or no detectable thermal effects caused by distant output transistors isolated by one or more other outputs. Tests were conducted with the device mounted on a typical PC board placed horizontally in a 33 cubic inch still air enclosure. The PC board was made of FR4 material measuring 2.5 by 2.5 inches, having double-sided circuit traces of 1.0 ounce copper soldered to each device pin. The board temperature was measured with thermal couple soldered to the board surface one inch away from the center of the device. The ambient temperature of the enclosure was measured with a second thermal couple located over the center of one inch distance from device.

THERMAL PERFORMANCE

Figure 22 illustrates the worst case thermal component parameters values for the 33291 in the 24-lead SOIC wide body surface mount package. Pins 5, 6, 7, 8, 17, 18, 19, and 20 of the package were connected directly to the lead frame flag. The parameter values indicated take into account adjacent output combinations. The characterization was conducted over power dissipation levels of 0.7 W to 17 W. The junction-to-ambient temperature resistance was found to be 40°C/W with a single output active (34°C/W with all outputs dissipating equal power 0 and the thermal resistance from junction-to-PC board ($R_{JUNCTION-BOARD}$) to be 30°C/W (board temperature, measure one inch from device center). The junction-to-heatsink lead resistance was found again to approximate 10°C/W. Devoting additional PC board metal around the heatsinking pins for this package improved the R_{PKG} from 33° to 31°C/W.

The total power dissipation available is dependent on the number of outputs enabled at any one time. At 25°C the $R_{DS(ON)}$ in 450 mΩ with a coefficient of 6500 ppm/°C. For the junction temperature to remain below 150°C, the maximum available power dissipation must decrease as the ambient temperature increases. Figure 23 depicts the per output limit of current at ambient temperatures necessary when one, four, or eight outputs are enable ON. Figure 25 illustrates how the $R_{DS(ON)}$ output value is affected by junction temperature.



Package	Rdx (Ω)*	C_{dx} (F)*	R_{pkg} (Ω)*	C_{pkg} (F)*
24-Lead SOIC	7.0	0.002	33	0.15

* Ω = °C/W, F = W s/°C, I_{PWR} = W, and V_A = °C

Figure 22. Thermal Model (Electrical Equivalent)

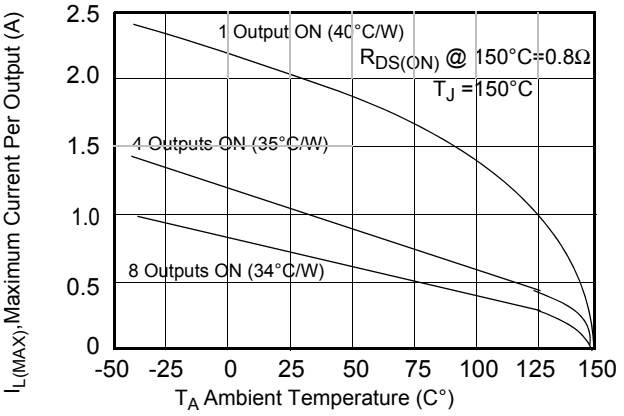


Figure 23. Maximum SOIC Package Steady State Output Current vs. Ambient Temperature

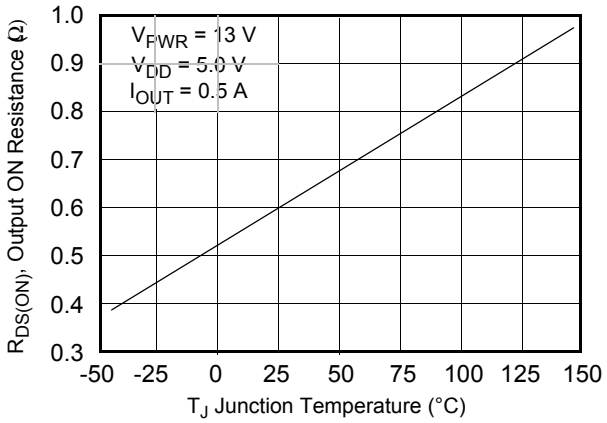


Figure 25. Maximum Output ON Resistance vs. Junction Temperature

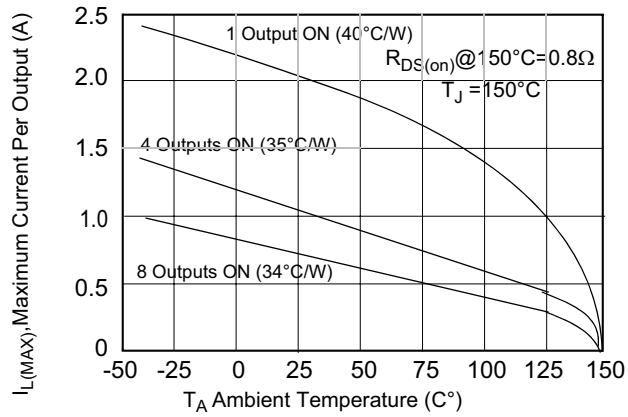
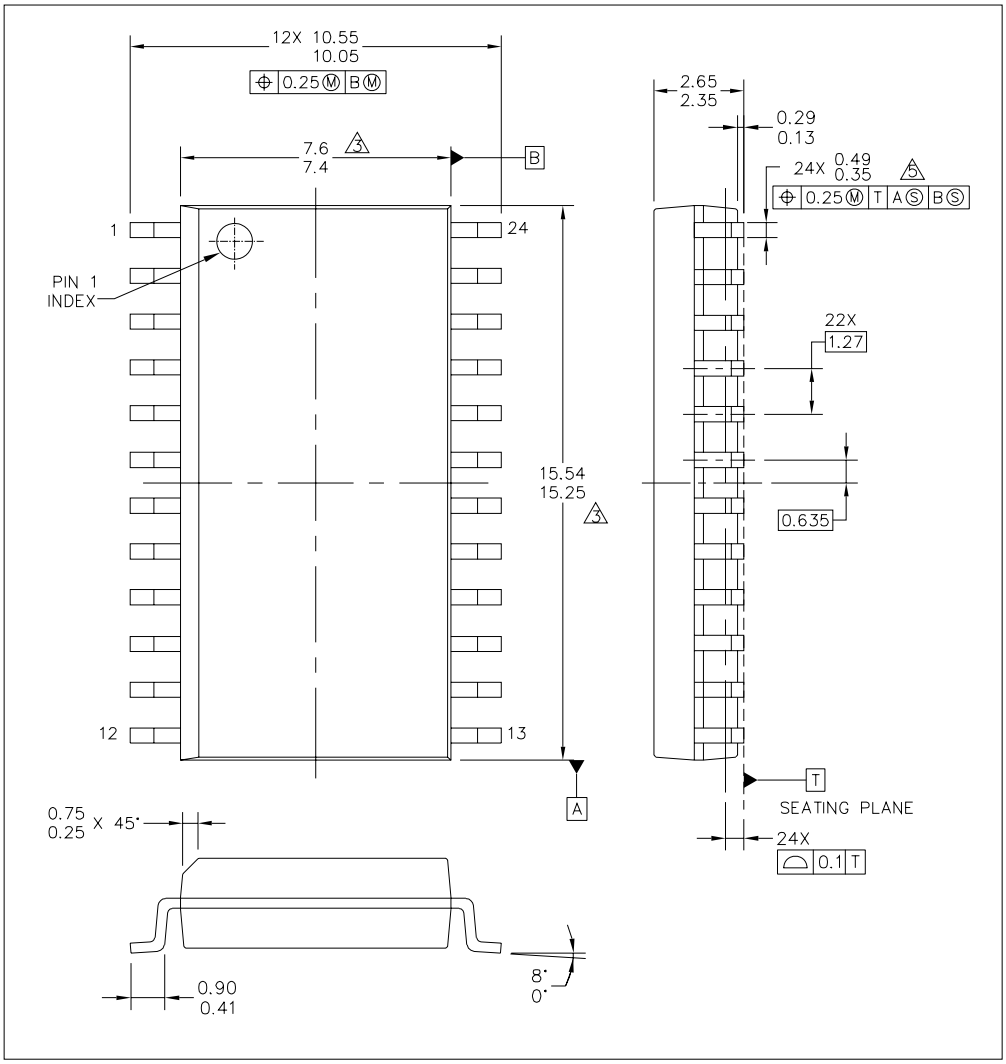


Figure 24. Maximum SOP Package Steady State Output Current vs. Ambient Temperature

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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TITLE: 24LD SOIC W/B, 1.27 PITCH 7.5 X 15.4 CASE–OUTLINE	DOCUMENT NO: 98ASB42344B	REV: G
	CASE NUMBER: 751E–05	05 DEC 2007
	STANDARD: JEDEC MS–013 AD	

DW SUFFIX
EG SUFFIX PB-FREE)
24-PIN
98ASB42344B
ISSUE G

33291

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. THIS DIMENSION DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15(0.006) PER SIDE.
5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13(0.005) TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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DW SUFFIX
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24-PIN
98ASB42344B
ISSUE G

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	8/2006	• Implemented Revision History page • Converted to Freescale format and prevailing form and style • Added EPP prefix Z to EG suffix device • Removed MC33291EG/R2 and replaced with MCZ33291EG/R2 in the Ordering Information block
4.0	10/2006	• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 4. Added note with instructions to obtain this information from www.freescale.com.
5	7/2008	• Corrected cross references throughout document • Updated Outline drawing to new revision “G”

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